CLAIMS

What is claimed is:

- A semiconductor device comprising:
 at least one layer of boro-phospho silicate glass; and
 at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of the at least one layer of boro-phospho silicate glass.
- 2. A semiconductor device comprising:
 a plurality of layers of boro-phospho silicate glass; and
 a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one
 layer of said plurality of layers of germanium boro-phospho silicate glass contacting at
 least a portion of at least one layer of said plurality of layers of boro-phospho silicate
 glass.
- 3. A semiconductor device comprising:
 a plurality of layers of boro-phospho silicate glass; and
 a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.
- 4. A semiconductor memory device comprising:
 at least one layer of boro-phospho silicate glass; and
 at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of the at least one layer of boro-phospho silicate glass.

- 5. A semiconductor memory device comprising:
- a plurality of layers of bord-phospho silicate glass; and
- a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.
- 6. A semiconductor memory device comprising:
 a plurality of layers of boro-phospho silicate glass; and
 a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.
- 7. A semiconductor memory device comprising: at least one capacitor cell having a portion thereof formed by at least one layer of boro-phospho silicate glass and at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of the at least one layer of borophospho silicate glass.
- 8. A semiconductor memory device comprising:
 at least one capacitor cell having a portion thereof formed by a plurality of layers of borophospho silicate glass and a plurality of layers of germanium borophospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium borophospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

- 9. A semiconductor memory device comprising: at least one capacitor dell having a portion thereof formed by a plurality of layers of borophospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of borophospho silicate glass.
- 10. The memory device of claim 9, further comprising: at least one dielectric layer; and a conductive layer over the at least one dielectric layer.

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- 11. The memory device of claim 10, wherein the at least one dielectric layer comprises one of Si_3N_4 , Ta_2O_5 , and BST.
 - 12. The memory device of claim 10, wherein the conductive layer comprises Si-Ge.
- 13. The memory device of claim 9, further comprising: at least one dielectric layer covering at least portions of the plurality of layers of boro-phospho silicate glass and the plurality of layers of germanium boro-phospho silicate glass; and a conductive layer covering at least a portion of the at least one dielectric layer.